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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,755	01/17/2002	Haruo Shoji	100353-00092	2653

7590 09/02/2005

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EXAMINER
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BAKER, PAUL A

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/046,755	<b>Applicant(s)</b> SHOJI, HARUO	
	<b>Examiner</b> Paul A. Baker	<b>Art Unit</b> 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) 6 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5,7,8 and 10-14 is/are rejected.
- 7) ☒ Claim(s) 3,4 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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### **DETAILED ACTION**

Prosecution on the merits of this application is reopened on claims 1, 2, 5, 7, 8, 10-14 are considered unpatentable for the reasons indicated below:

Applicable art under 35 USC §102 has been discovered.

Allowance over intervening art of record Furuyama et al., US Patent 6,643,758 was improper since the applicant has not perfected the foreign priority of the present application. To perfect applicant's claim of foreign priority, applicant must submit an English translation of the certified copy along with a statement that the translation of the certified copy is accurate; see MPEP §201.15.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,2 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Cleveland et al., US Patent 6,567,289.

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In regards to claim 1, Cleveland discloses a semiconductor memory device (figure 3 element 300), comprising a plurality of areas (figure 3 element 302, each column is an area), each accommodating one or more small sectors in a predetermined physical address of each area, or in a series of a plurality of physical addresses including the predetermined physical address of the area (figure 3 elements 308A-D), said predetermined physical address being one of a highest physical address of the area and a lowest physical address of the area (column 3 lines 23-30).

In regards to claim 2, Cleveland discloses a plurality of sectors larger than one or more of the small sectors in each of the plurality of the areas (figure 3 element 302, each column is an area); and

an address-conversion circuit configured to perform conversion of a sector address inputted from an outside source to make the plurality of the areas function as the same boot block type (column 3 lines 23-30, address inputted from an outside source is inherent to Cleveland's invention since an address must be supplied in order to access the disclosed memory device).

In regards to claim 10, Cleveland discloses a method for converting an address, comprising:

connecting a conversion circuit (column 3 lines 23-30) to a semiconductor memory device having a plurality of areas, each having a plurality of sectors (figure 3 element 302); and

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converting a sector-address inputted from an outside source by the sector-address conversion circuit, so that the semiconductor memory device functions as a same boot block type, wherein the sector address inputted may address any one of the plurality of sectors in the memory device (column 3 lines 23-30).

Claims 1, 2, 5, 7, 8, 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Furuyama et al. US Patent 6,643,758. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

In regards to claim 1, Furuyama discloses a semiconductor memory device (figure 4), comprising a plurality of areas (figure 4 elements 10A-D), each accommodating one or more small sectors in a predetermined physical address of each area, or in a series of a plurality of physical addresses including the predetermined physical address of the area (figure 4 elements 10A&D vs. elements 10B&C), said predetermined physical address being one of a highest physical address of the area and a lowest physical address of the area (figure 1 sub-figures 1 and 2).

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In regards to claim 2, Furuyama discloses a plurality of sectors larger than one or more of the small sectors in each of the plurality of the areas (figure 4 elements 10B-C); and

an address-conversion circuit configured to perform conversion of a sector address inputted from an outside source to make the plurality of the areas function as the same boot block type (in figures 7A-B).

In regards to claim 5, Furuyama discloses the semiconductor device is capable of storing one of a rewriting program or a boot program into one or more small sectors at a time in column 5 lines 59-62.

In regards to claim 7, Furuyama discloses in figures 7A&B a sector address conversion circuit comprising:

a sector-address input terminal (signals A18,A19);

a sector-address output terminal (TB19-TB20);

a boot block type specifying terminal that specifies a desired boot block type of a memory device having a plurality of sectors (TBBLKB); and

a signal conversion circuit that converts a sector address inputted to the sector-address input terminal based on a signal inputted to the boot block type specifying terminal and a most significant bit of the sector address, and outputs a converted sector address from the sector-address output terminal, so that the semiconductor memory device functions as a desired boot block type (elements 40-48) , wherein the sector address inputted may address any one of the plurality

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of sectors in the memory device (all addresses are converted via address conversion circuit in figures 7A-B).

In regards to claim 8, Furuyama discloses a control circuit for controlling the semiconductor memory device, which specifies a boot block type by providing a command (figure 4 element 18).

In regards to claim 10, Furuyama discloses a method for converting an address, comprising:

connecting a conversion circuit to a semiconductor memory device (figure 4 element 22) having a plurality of areas (figure 4 elements 10A-D), each having a plurality of sectors (figure 3); and

converting a sector-address inputted from an outside source by the sector-address conversion circuit, so that the semiconductor memory device functions as a same boot block type (in figures 7A-B) , wherein the sector address inputted may address any one of the plurality of sectors in the memory device (all addresses are converted via address conversion circuit in figures 7A-B).

In regards to claim 11, Furuyama discloses each of the plurality of sectors can be changed to be a top or bottom boot block type (column 6 lines 36-41).

In regards to claim 12, Furuyama discloses the sector-address conversion circuit changes the memory address to one of a top or bottom type (figures 7A-B).

In regards to claim 13, Furuyama discloses each of the plurality of sectors can be changed to be a top or bottom boot block type (column 6 lines 36-41).

In regards to claim 14, Furuyama discloses in figures 7A-B a sector-address conversion circuit, comprising:

- a sector-address input terminal (signals A18-A19);

- a sector-address output terminal (TB19-TB20);

- two boot block type specifying terminals receiving internal signals to change a sector of a memory device to be a top or bottom boot block type (element 44 and figure 7B signal A18); and

- a signal conversion circuit that conveys a sector address inputted to the sector-address input terminal based on a signal inputted to one of the boot block type specifying terminals and a most significant bit of the sector address, and outputs a converted sector address from the sector-address output terminal, so that the semiconductor memory device functions as a desired boot block type (elements 40-48), , wherein the sector address inputted may address any one of the plurality of sectors in the memory device (all addresses are converted via address conversion circuit in figures 7A-B).



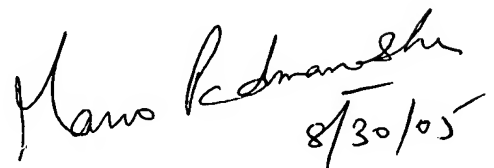
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Baker whose telephone number is (571)272-4203. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB



**MANO PADMANABHAN**  
**SUPERVISORY PATENT EXAMINER**